

## Assignment #5 Solutions

CENG 355

1. An SCI receiver (not necessarily an HC11 CSI receiver) samples the input at 16 times the bit rate of the receiver. The protocol has 1 start bit, 8 data bits and 1 stop bit. 3 samples are normally taken in the middle of each bit to determine if a bit is a 0 or a 1. How much faster can the receiver bit rate be compared to the transmitter bit rate to still have error free communication?

Soln: When the receiver clock runs too fast the first of the three samples of the stop bit may in fact sample the last data bit. If majority voting is used this will not give an error. If however the middle sample bit samples the last data bit rather than the stop bit an error may result. Let  $T_t$  be the period of the transmitter clock. Let  $T_{rmin}$  be the period of the receiver clock where the middle sample bit just samples the eighth data bit. Therefore

$$9T_t = 9T_{rmin} + 8/16T_{rmin}$$

Therefore  $T_t/T_{rmin} = 152/144$

$$\% \text{ faster} = [(F_r - F_t)/F_t]100 = [(1/T_{rmin} - 1/T_t)/(1/T_t)]100 = 5.55\%$$

2. Consider a 4 bit charge redistribution A/D where a least significant bit represents 0.5 volts. If the A/D structure and control algorithm as given in the course pack are used, what digital value is obtained for an analog input of 3.77 volts? What is the error for this conversion? What is the maximum error that would ever be obtained with this algorithm? If  $1/2$  of a least significant bit voltage is added to the analog voltage before it is sampled, what would the maximum error be?

Soln:  $V_{ref} = 8$  volts, therefore

$$v = 4a_3 + 2a_2 + a_1 + .5a_0 - 3.77$$

Therefore  $\{a_3, a_2, a_1, a_0\} = \{0, 1, 1, 1\}$  and the error is  $-.27$  volts.

The maximum error is  $.5$  volts.

If  $.25$  volts is added to the voltage to be converted the maximum error would be  $.25$  volts. In this example the equation used for successive approximation would be

$v = 4a_3 + 2a_2 + a_1 + .5a_0 - 4.02$  and the converted string would be  $\{1000\}$ . The error is now  $+.23$  volts.

3. What are the key features of the HC11 A/D subsystem?

Soln: 1. 8 bit charge redistribution successive approximation converter  
2.  $<1/2$  LSB error  
3. 8 external channels plus some internal channels  
4. always samples 4 consecutive channels or the same channel 4 times  
5. conversion complete flag but no interrupt upon completion.

4. In 2 or 3 concise sentences describe how portC handshaking works in the HC11.

Soln: The STRB output of the transmitter acts as a ready line and drives the STRA input of the receiver. The STRB output of the receiver acts as an acknowledge line and drives the STRA input of the transmitter. Writing data to the PORTCL register of the transmitter asserts ready whereas reading PORTCL of the receiver asserts acknowledge. Assertion of STRA at the transmitter deasserts ready whereas assertion of STRA at the receiver deasserts acknowledge and strobes new data into PORTCL. (It took me four sentences)

5. List in short point form the key features of the HC11 SCI receiver.

Soln: 1. uses nonreturn-to-zero asynchronous serial protocol with 1 start bit, 8 or 9 data bits and 1 stop bit.  
2. transmitter has data register empty and conversion complete flags and interrupts  
3. receiver has data register full, idle and overrun flags and interrupts