

Assignment 4

CENG 355

1. A 3 operand add instruction uses the addressing mode $M[M[R]+offset]$ for each operand. The op-code and offset are each 2 bytes, the machine has 256 registers and all addresses and data are 64 bits. How many bytes must be read and written from memory to process the instruction?
2. A computer uses a 32 bit address bus. Design complete address decoding to divide the address space into 32MB blocks. Design complete address decoding to divide a 32 MB block into 1MB blocks. Design linear address decoding to divide a 1MB block into 4KB blocks. Design complete address decoding to divide a 4KB block into 64B blocks.
3. Give the memory map for a 64K address space divided into 4K blocks with linear address decoding.
4. Design a complete address decoder for an 8B controller chip to be used with a M68000. The chip has 3 address lines, 2 asserted high chip select lines and 2 asserted low chip select lines.