**Assignment #5 Solutions CENG 355**

1. The time to access a byte from a cache is 20ns. The time to access a byte from the memory is 100ns. A write back policy is used. The line size is 64 bytes. The hit ratio is .998. What is the effective access time of the cache/memory system? What hit ratio is required for the cache based system to be faster than not using a cache? What assumptions are you making?

Soln: Assume entire line must be transferred to the cache before a miss can be completed. Therefore

$t_{effective\ access}$= .998x20 + .002x120x128 = 50.68ns

For the cache based system to be the same speed as a cacheless system

100 = hx20 + (1-h)x120x128
Therefore h = .9947849 where h is the hit ratio

2. A direct mapped16KB cache uses 128B/ line. If byte addresses are 32 bits, how is an address divided into fields? How many overhead bits does the cache require?

Soln: A 16KB cache with 128B/line has 2*7=128 frames. Therefore 7 bits are used as an index, 7 bits to address a byte within a line(the offset) and 18 bits for a tag. The number of overhead bits is 19 x 128 = 2432. The 19 is made up of 18 tag bits and 1 valid bit.

3. A 4 way set associative16KB cache uses 128B/ line. If byte addresses are 32 bits, how is an address divided into fields? How many overhead bits does the cache require?

Soln: The cache is divided into 4 subcaches each consisting of 32 frames. Therefore 5 bits are used for the index, 7 bits for the offset abd 20 bits for the tag. The number of overhead bits assuming random selection of a frame at an index is 1 for the valid bit + 20 for the tag x 32 x4= 21x128= 2688. If a least recently used (LRU) replacement algorithm is used to select a frame at an index, one could use an additional bit to the valid bit so that (2+20)x128=2816 overhead bits would be required.

4. A fully asociative16KB cache uses 128B/ line. If byte addresses are 32 bits, how is an address divided into fields? How many overhead bits does the cache require?

Soln: An address would consist of 7 offset bits and 25 tag bits. There would be 128 frames for data and a 26 x128 associative memory for overhead information if a random replacement algorithm is used. The 26 bits required for each frame consist of 1 valid bit and 25 tag bits. The total number of overhead bits would be 26 x128 = 3328. If an LRU replacement algorithm is used additional bits would be required to keep track of the least recently used frame.